1. Which of the following is the smallest entity of memory?

(a) Block  
(b) Cell  
(c) Instance  
(d) Set

Answer: (b),

2. The primary memory (also called main memory) of a personal computer consists of

(a) RAM only  
(b) ROM only  
(c) both RAM and ROM  
(d) Cache memory

Answer: (c)

3. The Boot sector files of the system are stored in which computer memory?

(a) RAM  
(b) ROM  
(c) Cache  
(d) Register

Answer: (b),

4. Which of the following statements are not correct about the main memory of a computer?

(a) In main memory, data gets lost when power is switched off.  
(b) Main memory is faster than secondary memory but slower than registers.  
(c) They are made up of semiconductors.  
(d) All are correct

Answer: (d)

5. RAM is \_ \_ \_ \_ \_ \_ and \_ \_ \_ \_ \_.

(a) volatile, temporary  
(b) non-volatile, temporary  
(c) volatile, permanent

(d) non-volatile, permanent

Answer: (a),

6. Which of the following is the lowest in the computer memory hierarchy?

(a) Cache  
(b) RAM  
(c) Secondary memory  
(d) CPU registers

Answer: (c)

7. Which of the following has the fastest speed in the computer memory hierarchy?

(a) Cache  
(b) Register in CPU  
(c) Main memory  
(d) Disk cache

Answer: (b)

 8. Which memory acts as a buffer between CPU and main memory?

(a) RAM  
(b) ROM  
(c) Cache  
(d) Storage

Answer: (c)

9.  Which process is used to map logical addresses of variable length onto physical memory?

(a) Paging  
(b) Overlays  
(c) Segmentation  
(d) Paging with segmentation

Answer: (c)

10.  Which of the following is used to transfer data between the processor (CPU) and memory?

(a) Cache  
(b) TLB  
(c) Buffer  
(d) Registers

Answer: (d)

11. . Which computer memory chip allows simultaneous both read and write operations?

(a) ROM  
(b) RAM  
(c) PROM  
(d) EEPROM

Answer: (b)

12. In which type of memory, once the program or data is written, it cannot be changed?

(a) EPROM  
(b) PROM  
(c) EEPROM  
(d) None of these

Answer: (b)

 13. In which type of ROM, data can be erased by ultraviolet light and then reprogrammed by the user or manufacturer?

(a) PROM  
(b) EPROM  
(c) EEPROM  
(d) Both a and b

Answer: (b)

14. Which type of ROM is used for erasing purposes only?

(a) PROM  
(b) EPROM  
(c) EEPROM  
(d) Both b and c

Answer: (c)

15. How many types of RAM are available?

(a) 4  
(b) 3  
(c) 2  
(d) 5

Answer: (c)

16.Auxillary memory access time is generally \_\_\_\_\_\_\_\_ times that of the main memory

A. 10  
B. 100  
C. 1000  
D. 10000

View Answer

Ans : C

17. What is the formula for Hit Ratio?

A. Hit/(Hit + Miss)  
B. Miss/(Hit + Miss)  
C. (Hit + Miss)/Miss  
D. (Hit + Miss)/Hit

View Answer

Ans : A

18. Which of the following is correct example for Auxiliary Memory?

A. Magnetic disks  
B. Tapes  
C. Flash memory.  
D. Both A and B

View Answer

Ans : D

19.  The next level of memory hierarchy after the L2 cache is \_\_\_\_\_\_\_

A. Secondary storage  
B. Main memory  
C. Register  
D. TLB

View Answer

Ans : C

20.  In how many categories memory/storage is classified?

A. 2  
B. 3  
C. 4  
D. 5

View Answer

Ans : A

21.  Which of the following is correct refreshed rate for DRAM?

A. 10~1000 ms  
B. 10~50 ms  
C. 10~100 ms  
D. 10~500 ms

View Answer

Ans : C

22. . Which of the following is true?

A. To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.  
B. If we use the flash drives instead of the harddisks, then the secondary storage can go above primary memory in the hierarchy.  
C. In the memory hierarchy, as the speed of operation increases the memory size also increases.  
D. Both A and C

View Answer

Ans : A

23.  Which of the following statement is/are true about static RAM?

(a) In static RAM, data is stored in flip flop.  
(b) It does not need to be refreshed periodically.  
(c) It is faster than dynamic RAM.  
(d) All of these are true.

Answer: (d)

24.  Which of the following chips stores the basic input-output system (BIOS)?

(a) RAM  
(b) ROM  
(c) PROM  
(d) None of these

Answer: (b)

25.  Which of the following statement is false about dynamic RAM?

(a) DRAM needs a continuously refreshed memory to store data.  
(b) It is slower than SRAM.  
(c) It is more expensive than SRAM.  
(d) All are correct.

Answer: (c)

26. Which of the following statement is/are true about static RAM?

(a) In static RAM, data is stored in flip flop.  
(b) It does not need to be refreshed periodically.  
(c) It is faster than dynamic RAM.  
(d) All of these are true.

Answer: (d)

27.  SDRAM stands for

(a) Static DRAM  
(b) Synchronous DRAM  
(c) Super DRAM  
(d) Semi DRAM

Answer: (b)

28. Which of the following is not RAM?

(a) SRAM  
(b) DRAM  
(c) WRAM and VRAM  
(d) PRAM

Answer: (d)

29. Virtual memory is an

(a) extremely large memory  
(b) extremely large secondary memory  
(c) illusion of an extremely large memory  
(d) a type of memory used in supercomputers.

Answer: (c)

30. The memory that cannot be accessed directly by processor (CPU) is

(a) internal memory  
(b) external memory  
(c) cache memory  
(d) system memory

Answer: (b)

31. Higher the RAM of computer, the faster its processing speed. Since it eliminates

(a) need for external memory  
(b) need for ROM  
(c) need for cache memory  
(d) All of these

Answer: (a)

32.  What happens when RAM is full in the computer?

(a) Cache memory is used  
(b) The volatile memory is used  
(c) An interrupt is raised  
(d) Hard disk is used

Answer: (b)

33. Storage that stores or retains data/information permanently after power off is called

(a) Volatile storage  
(b) Non-volatile storage  
(c) Sequential storage  
(d) Both a and b

Answer: (b)

34.  Brain of computer is \_\_\_\_\_\_\_\_\_\_\_\_

A. Control unit  
B. Arithmetic and Logic unit  
C. CPU  
D. Memory

View Answer

Ans : C

35. Causing the CPU to step through a series of micro operations is called \_\_\_\_\_\_\_\_\_

A. Execution  
B. Runtime  
C. Pipelining  
D. Sequencing

View Answer

Ans : D

36. To resolve the clash over the access of the system BUS we use \_\_\_\_\_\_

   **A.)** BUS arbitrator

   **B.)**Multiple BUS

   **C.)**Priority access

   **D.)**None of the above

**Show Answer**

**Answer: Option 'A'**

37.  BUS arbitration approach uses the involvement of the processor.

   **A.)** Centralised arbitration

   **B.)**Distributed arbitration

   **C.)**Random arbitration

   **D.)**All of the above

**Show Answer**

**Answer: Option 'A'**

38. The device which is allowed to initiate data transfers on the BUS at any time is called \_\_\_\_\_

   **A.)** Controller

   **B.)**BUS arbitrator

   **C.)**BUS master

   **D.)**Processor

**Show Answer**

**Answer: Option 'C'**

39. The Centralised BUS arbitration is similar to \_\_\_\_\_\_ interrupt circuit.

   **A.)** Priority

   **B.)**Parallel

   **C.)**Single

   **D.)**Daisy chain

**Show Answer**

**Answer: Option 'D'**

40. When the processor receives the request from a device, it responds by sending \_\_\_\_\_\_\_\_\_\_\_.

   **A.)** Acknowledge signal

   **B.)**BUS grant signal

   **C.)**Response signal

   **D.)**None of the above

**Show Answer**

**Answer: Option 'B'**

41. In Centralised Arbitration \_\_\_\_\_\_ is/are is the BUS master.

   **A.)** Processor

   **B.)**DMA controller

   **C.)**Device

   **D.)**Both Processor and DMA controller

**Show Answer**

**Answer: Option 'D'**

41. The BUS busy line is made of \_\_\_\_\_\_\_\_

   **A.)** Open-drain circuit

   **B.)**Open-collector circuit

   **C.)**EX-Or circuit

   **D.)**Nor circuit

**Show Answer**

**Answer: Option 'B'**

42. The BUS busy line is used \_\_\_\_\_\_\_\_\_\_

   **A.)** To indicate the processor is busy

   **B.)**To indicate that the BUS master is busy

   **C.)**To indicate the BUS is already allocated

   **D.)**None of these

**Show Answer**

**Answer: Option 'C'**

43. Distributed arbitration makes use of \_\_\_\_\_\_

   **A.)** BUS master

   **B.)**Processor

   **C.)**Arbitrator

   **D.)**4-bit ID

**Show Answer**

**Answer: Option 'D'**

44.   
If two devices A and B contesting for the BUS have ID’s 5 and 6 respectively, which device gets the BUS based on the Distributed arbitration.

   **A.)** Device A

   **B.)**Device B

   **C.)**Insufficient information

   **D.)**None of the above

**Show Answer**

**Answer: Option 'B'**

45.   
The DMA transfer is initiated by \_\_\_\_\_

   **A.)** Processor

   **B.)**The process being executed

   **C.)**I/O devices

   **D.)**OS

**Show Answer**

**Answer: Option 'C'**

46. The technique whereby the DMA controller steals the access cycles of the processor to operate is called \_\_\_\_\_\_\_\_\_\_

   **A.)** Fast conning

   **B.)**Memory Con

   **C.)**Cycle stealing

   **D.)**Memory stealing

**Show Answer**

**Answer: Option 'C'**

47.   
When the R/W bit of the status register of the DMA controller is set to 1.

   **A.)** Read operation is performed

   **B.)**Write operation is performed

   **C.)**Read & Write operation is performed

   **D.)**None of the above

**Show Answer**

**Answer: Option 'A'**

48. The DMA controller has \_\_\_\_\_\_\_ registers.

   **A.)** 4

   **B.)**3

   **C.)**2

   **D.)**1

**Show Answer**

**Answer: Option 'B'**

49. The DMA transfers are performed by a control circuit called as \_\_\_\_\_\_\_\_\_\_

   **A.)** Device interface

   **B.)**DMA controller

   **C.)**Data controller

   **D.)**Overlooker

**Show Answer**

**Answer: Option 'B'**

50. The DMA differs from the interrupt mode by \_\_\_\_\_\_\_\_\_\_

   **A.)** The involvement of the processor for the operation

   **B.)**The method of accessing the I/O devices

   **C.)**The amount of data transfer possible

   **D.)**None of the above

**Show Answer**

**Answer: Option 'D'**

51.  is used as an intermediate to extend the processor BUS.

   **A.)** Bridge

   **B.)**Router

   **C.)**Connector

   **D.)**Gateway

**Show Answer**

**Answer: Option 'A'**

52.   
The classification of BUSes into synchronous and asynchronous is based on \_\_\_\_\_\_\_\_\_\_

   **A.)** The devices connected to them

   **B.)**The type of data transfer

   **C.)**The Timing of data transfers

   **D.)**None of these

**Show Answer**

**Answer: Option 'C'**

53. The device which starts data transfer is called \_\_\_\_\_\_\_\_\_\_

   **A.)** Master

   **B.)**Transactor

   **C.)**Distributor

   **D.)**Initiator

**Show Answer**

**Answer: Option 'D'**

54. .

In synchronous BUS, the devices get the timing signals from \_\_\_\_\_\_\_\_\_\_

   **A.)** Timing generator in the device

   **B.)**A common clock line

   **C.)**Timing signals are not used at all

   **D.)**None of these

**Show Answer**

**Answer: Option 'B'**

55. The delays caused in the switching of the timing signals is due to \_\_\_\_\_\_\_\_\_\_

   **A.)** Memory access time

   **B.)**WMFC

   **C.)**Propagation delay

   **D.)**Processor delay

**Show Answer**

**Answer: Option 'C'**

56. .

Which is fed into the BUS first by the initiator?

   **A.)** Data

   **B.)**Address

   **C.)**Commands or controls

   **D.)**Address, Commands or controls

**Show Answer**

**Answer: Option 'D'**

57. signal is used as an acknowledgement signal by the slave in Multiple cycle transfers.

   **A.)** Ack signal

   **B.)**Slave ready signal

   **C.)**Master ready signal

   **D.)**Slave received signal

**Show Answer**

**Answer: Option 'B'**

58. The transmission on the asynchronous BUS is also called \_\_\_\_\_

   **A.)** Switch mode transmission

   **B.)**Hand-Shake transmission

   **C.)**Variable transfer

   **D.)**Bulk transfer

**Show Answer**

**Answer: Option 'B'**

59. MRDC stands for \_\_\_\_\_\_\_

   **A.)** Memory Read Enable

   **B.)**Memory Ready Command

   **C.)**Memory Re-direct Command

   **D.)**None of the above

**Show Answer**

**Answer: Option 'B'**

60. The status flags required for data transfer is present in \_\_\_\_\_

   **A.)** Device

   **B.)**Device driver

   **C.)**Interface circuit

   **D.)**None of these

**Show Answer**

**Answer: Option 'C'**

**Question 1:** What is the primary function of the processing unit in a computer? A) Store data and information B) Perform calculations and make decisions C) Manage input and output devices D) Establish network connections

**Answer:** B) Perform calculations and make decisions

**Question 2:** Which component of the processing unit is responsible for performing arithmetic and logical operations? A) ALU (Arithmetic Logic Unit) B) CU (Control Unit) C) Memory Unit D) Input Unit

**Answer:** A) ALU (Arithmetic Logic Unit)

**Question 3:** What is the role of the Control Unit (CU) in the processing unit? A) It performs arithmetic operations. B) It manages input and output devices. C) It controls the flow of data and instructions within the computer. D) It stores temporary data for quick access.

**Answer:** C) It controls the flow of data and instructions within the computer.

**Question 4:** Which of the following is a component of the CPU responsible for fetching and decoding instructions? A) ALU (Arithmetic Logic Unit) B) Cache Memory C) Control Unit (CU) D) RAM (Random Access Memory)

**Answer:** C) Control Unit (CU)

**Question 5:** What is the purpose of the ALU (Arithmetic Logic Unit) in the processing unit? A) It stores data and instructions for future use. B) It performs arithmetic and logical operations on data. C) It manages input and output devices. D) It controls the flow of data within the computer.

**Answer:** B) It performs arithmetic and logical operations on data.

**Question 6:** Which term refers to the speed at which the processor executes instructions? A) Clock Speed B) Bit Rate C) Cache Size D) RAM Capacity

**Answer:** A) Clock Speed

**Question 7:** What is the function of the CPU cache memory? A) Store frequently accessed data and instructions for faster processing B) Manage input and output devices C) Perform arithmetic calculations D) Control the flow of data within the computer

**Answer:** A) Store frequently accessed data and instructions for faster processing

**Question 8:** Which technology allows a processor to work on multiple tasks simultaneously? A) Multi-core processing B) Overclocking C) Thermal throttling D) Hyperthreading

**Answer:** A) Multi-core processing

**Question 9:** What is the main purpose of the CPU's heat sink and fan? A) Increase the clock speed of the processor B) Reduce the size of the processor C) Dissipate heat generated by the processor D) Improve the processor's calculation accuracy

**Answer:** C) Dissipate heat generated by the processor

**Question 10:** Which unit of measurement is commonly used to express the speed of processors? A) Megabytes (MB) B) Gigahertz (GHz) C) Terabytes (TB) D) Kilobits (Kb)

**Answer:** B) Gigahertz (GHz)

**Question 1:** What is microprogrammed control in computer architecture? A) A type of control unit that uses hardwired logic circuits B) A control unit that uses microinstructions to control the operations of the computer C) A type of memory used for data storage D) A peripheral device used for input and output operations

**Answer:** B) A control unit that uses microinstructions to control the operations of the computer

**Question 2:** What are microinstructions? A) High-level instructions executed by the CPU B) Low-level instructions used for programming microcontrollers C) Instructions used by the control unit to control the internal operations of the CPU D) Instructions used for input and output operations

**Answer:** C) Instructions used by the control unit to control the internal operations of the CPU

**Question 3:** In microprogrammed control, where are microinstructions stored? A) RAM (Random Access Memory) B) ROM (Read-Only Memory) C) Cache Memory D) Hard Disk Drive

**Answer:** B) ROM (Read-Only Memory)

**Question 4:** Which of the following is a characteristic of micro programmed control? A) Faster execution of instructions B) Easier modification and flexibility in changing control signals C) Limited control over the computer's operations D) Lower cost compared to hardwired control

**Answer:** B) Easier modification and flexibility in changing control signals

**Question 5:** What is the role of the control memory in microprogrammed control? A) Store data used by the CPU B) Store microinstructions that control the CPU's operations C) Store results of arithmetic operations D) Store the operating system software

**Answer:** B) Store microinstructions that control the CPU's operations

**Question 6:** What is a microprogram sequencer in microprogrammed control? A) A device that generates the control signals for the CPU B) A device that fetches microinstructions from memory C) A component that controls the flow of microinstructions during execution D) A type of secondary storage device

**Answer:** C) A component that controls the flow of microinstructions during execution

**Question 7:** Which of the following statements is true about microprogrammed control? A) It uses fixed, hardwired control circuits. B) It allows easy modification and updates to the control unit's behavior. C) It is slower than hardwired control. D) It cannot handle complex instructions.

**Answer:** B) It allows easy modification and updates to the control unit's behavior.

**Question 8:** What does a control word in microprogrammed control represent? A) A set of microinstructions B) A binary representation of an instruction C) A memory address in RAM D) A register in the CPU

**Answer:** A) A set of microinstructions

**Question 9:** Which one of the following is a disadvantage of microprogrammed control? A) Difficult modification of control signals B) Limited flexibility in handling complex instructions C) Slower execution of instructions compared to hardwired control D) Higher cost of implementation

**Answer:** C) Slower execution of instructions compared to hardwired control

**Question 10:** In microprogrammed control, what is a horizontal microinstruction? A) A microinstruction that specifies a single control signal B) A microinstruction that controls the sequencing of operations C) A microinstruction that controls data transfer between registers D) A microinstruction that handles input and output operations

**Answer:** A) A microinstruction that specifies a single control signal